AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a plurality of memory cells in a plurality of chip areas on a main surface of a semiconductor wafer, forming a plurality of multi-layered first wirings in an upper layer of said plurality of memory cells and forming a plurality of fuses in said plurality of chip areas during the step of forming said plurality of memory cells or the step of forming said plurality of first wirings;

(b) forming a passivation layer over said plurality of first wirings and said plurality of fuses, and removing parts of said passivation ~~layers~~ layer to expose a wiring in the same layer as the uppermost wiring of said plurality of first wirings, thereby forming a plurality of internal connection terminals;

(c) removing other parts of said passivation ~~layers~~ layer, thereby forming fuse openings over each of said plurality of fuses;

(d) after said step (b), conducting a probe test to detect presence of defect cells, and irradiating laser to ~~said~~ a fuse through a ~~predetermined~~ corresponding fuse opening of said plurality of fuse openings, thereby cutting said fuse by fusion when said probe test detects defect cells;

(e) after said step (d), forming an elastomer layer on said passivation layer, said passivation layer being formed also in said plurality of fuse openings;

(f) performing a heat treatment to said elastomer layer, thereby curing

said elastomer layer;

(g) forming a plurality of second wirings having one ends electrically connected to said internal connection terminals over said elastomer layer, then forming an uppermost protection layer on said plurality of second wirings and removing a part of said uppermost protection layer, thereby selectively exposing the other ends of said plurality of second wirings;

(h) performing a heat treatment to said uppermost protection layer, thereby curing said uppermost protection layer; and

(i) forming a plurality of external connection terminals at the other ends of said plurality of second wirings, then cutting said semiconductor wafer into said chip areas, thereby obtaining a plurality of semiconductor chips,

wherein a temperature of each of the heat treatments in said steps (f) and (h) is set at a certain temperature so as not to change ~~predetermined~~ characteristics of said plurality of memory cells.

2. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 1,

wherein a temperature of each of the heat treatments in said steps (f) and (h) is below 260°C.

3. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 1,

wherein said passivation layer includes an inorganic passivation layer and an organic passivation layer formed thereon, and said organic passivation layer is formed of an organic material, a layer of which is cured by a heat treatment.

4. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 3,

wherein said step of the heat treatment to said organic passivation layer is performed in advance of said step (d), and a temperature of the heat treatment of said organic passivation layer is higher than that of each of the heat treatments in said steps (f) and (h).

5. (Currently Amended) The method of manufacturing a semiconductor integrated circuit device according to claim 3,

wherein said step of the heat treatment to said organic passivation layer is performed after said step (d), and a temperature of the heat treatment of said organic passivation layer is set at a certain temperature so as not to change ~~predetermined~~ characteristics of said plurality of memory cells.

6. (Currently Amended) A method of manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a plurality of memory cells in a plurality of chip areas on a main surface of a semiconductor wafer, forming a plurality of multi-layered first wirings in an upper layer of said plurality of memory cells, and forming a plurality of fuses in said plurality of chip areas during the step of forming said plurality of memory cells or the step of forming said plurality of first wirings;

(b) forming a passivation layer over said plurality of first wirings and said plurality of fuses, and removing parts of said passivation ~~layers~~ layer to expose a wiring in the same layer as the uppermost wiring of said plurality of first wirings, thereby forming a plurality of internal connection terminals.

wherein said passivation layer includes an inorganic passivation layer and an organic passivation layer formed thereon, and said organic passivation layer is formed of an organic material, a layer of which is cured by a heat treatment;

(c) removing other parts of said ~~passivation layers~~ passivation layer, thereby forming fuse openings over each of said plurality of fuses;

(d) after said step (b), conducting a probe test to detect presence of defect cells, and irradiating laser to ~~said~~ a fuse through a ~~predetermined~~ corresponding fuse opening of said plurality of fuse openings, thereby cutting said fuse by fusion when said probe test detects defect cells;

(e) forming a plurality of second wirings having one ends electrically connected to said internal connection terminals over said passivation layer, then forming an uppermost protection layer on said plurality of second wirings and removing a part of said uppermost protection layer, thereby selectively exposing the other ends of said plurality of second wirings;

(f) performing a heat treatment to said uppermost protection layer, thereby curing said uppermost protection layer; and

(g) forming a plurality of external connection terminals at the other ends of said plurality of second wirings, then cutting said semiconductor wafer into said chip areas, thereby obtaining a plurality of semiconductor chips,

wherein a temperature of the heat treatment in said step (f) is set at a certain temperature so as not to change ~~predetermined~~ characteristics of said plurality of memory cells.

7. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 6,

wherein a temperature of the heat treatment in said step (f) is below 260°C.

Claim 8. (Canceled without prejudice or disclaimer).

9. (Currently Amended) The method of manufacturing a semiconductor integrated circuit device according to claim ~~8~~ 6,

wherein a temperature of the heat treatment of said organic passivation layer is higher than that of the heat treatment in said step (f).

10. (Original) The method of manufacturing a semiconductor integrated circuit device according to claim 6,

wherein at least a part of said plurality of second wirings are arranged over at least a part of said plurality of fuses.

11. (Currently Amended) The method of manufacturing a semiconductor integrated circuit device according to claim 6,

wherein said second ~~wiring is~~ wirings are formed of a conductive layer formed by a plating method.

12. (Currently Amended) The method of manufacturing a semiconductor integrated circuit device according to claim 6,

wherein said plurality of memory cells include a DRAM and a flash memory, ~~arid~~ and a retention bake of said flash memory is performed simultaneously with a

heat treatment of said organic passivation layer.

13. (New) A method of manufacturing a semiconductor integrated circuit device, comprising the steps of:

(a) forming a plurality of memory cells in a plurality of chip areas on a main surface of a semiconductor wafer, forming a plurality of multi-layered first wirings in an upper layer of said plurality of memory cells, and forming a plurality of fuses in said plurality of chip areas during the step of forming said plurality of memory cells or the step of forming said plurality of first wirings;

(b) forming a passivation layer over said plurality of first wirings and said plurality of fuses, and removing parts of said passivation layer to expose a wiring in the same layer as the uppermost wiring of said plurality of first wirings, thereby forming a plurality of internal connection terminals;

(c) removing other parts of said passivation layer, thereby forming fuse openings over each of said plurality of fuses;

(d) after said step (b), conducting a probe test to detect presence of defect cells, and irradiating laser to a fuse through a corresponding fuse opening of said plurality of fuse openings, thereby cutting said fuse by fusion when said probe test detects defect cells;

(e) forming a plurality of second wirings having one ends electrically connected to said internal connection terminals over said passivation layer, then forming an uppermost protection layer on said plurality of second wirings and removing a part of said uppermost protection layer, thereby selectively exposing the other ends of said plurality of second wirings,

wherein said second wirings are formed of a conductive layer formed by a

plating method;

(f) performing a heat treatment to said uppermost protection layer, thereby curing said uppermost protection layer; and

(g) forming a plurality of external connection terminals at the other ends of said plurality of second wirings, then cutting said semiconductor wafer into said chip areas, thereby obtaining a plurality of semiconductor chips;

wherein a temperature of the heat treatment in said step (f) is set at a certain temperature so as not to change characteristics of said plurality of memory cells.